Single Slope ADC in FPGA for mu2e

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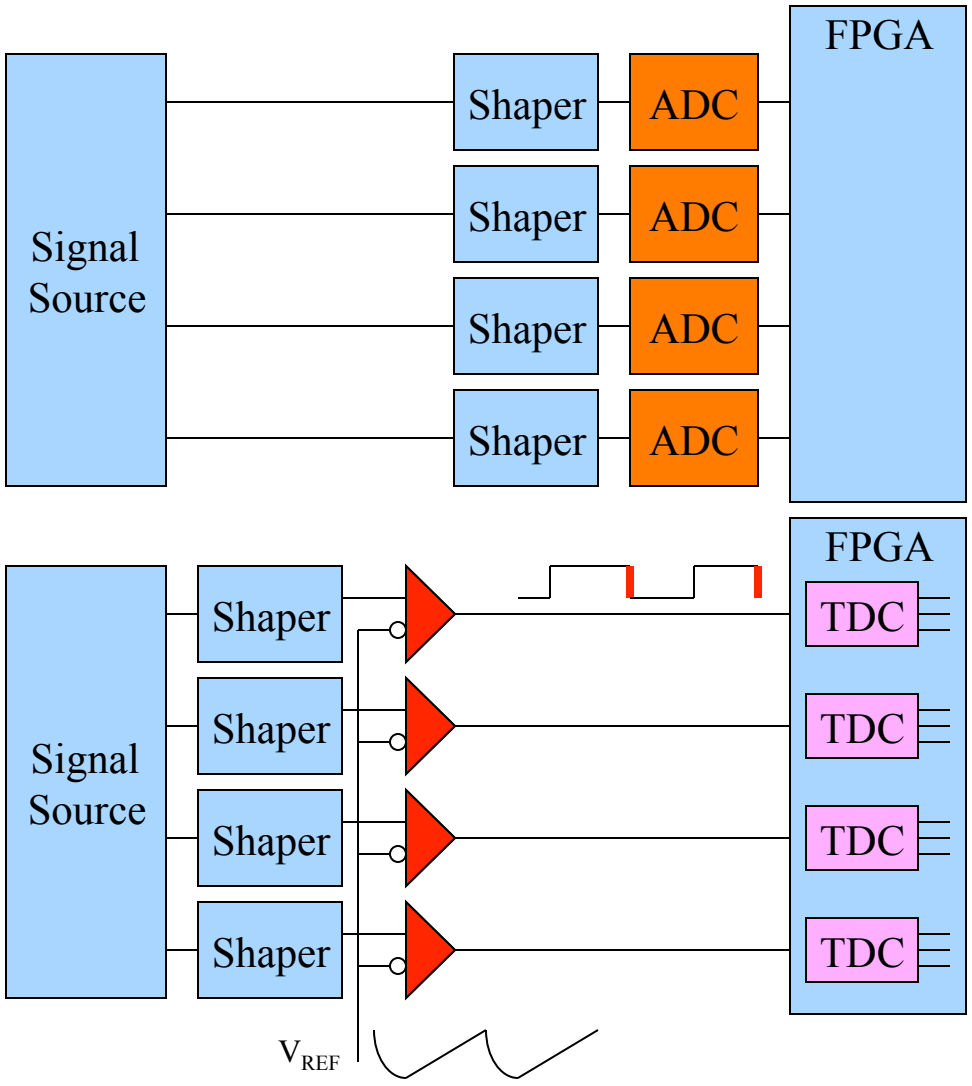
Introduction

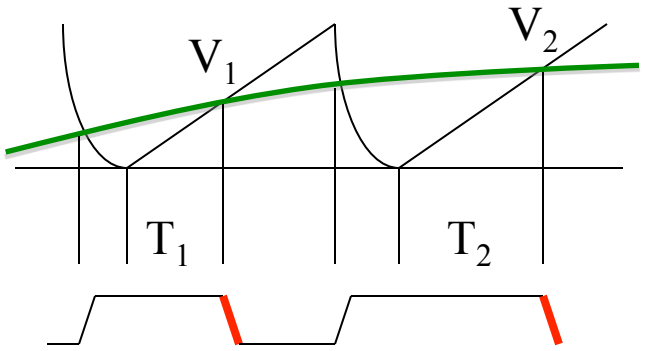
- We already have a 16-channel Wave Union TDC firmware that has been implemented in an Altera Cyclone III FPGA device (EP3C25F324C6N, $73.90) and has been tested on a Cyclone III evaluation card.
- The same device can fit 32 channels.
- The power consumption is as low as 27 mW/ channel (with 32 channels/device).
- The same TDC can be used as an ADC with a ramping reference added to the front-end for analog-to-time conversion.

Using FPGA as ADC

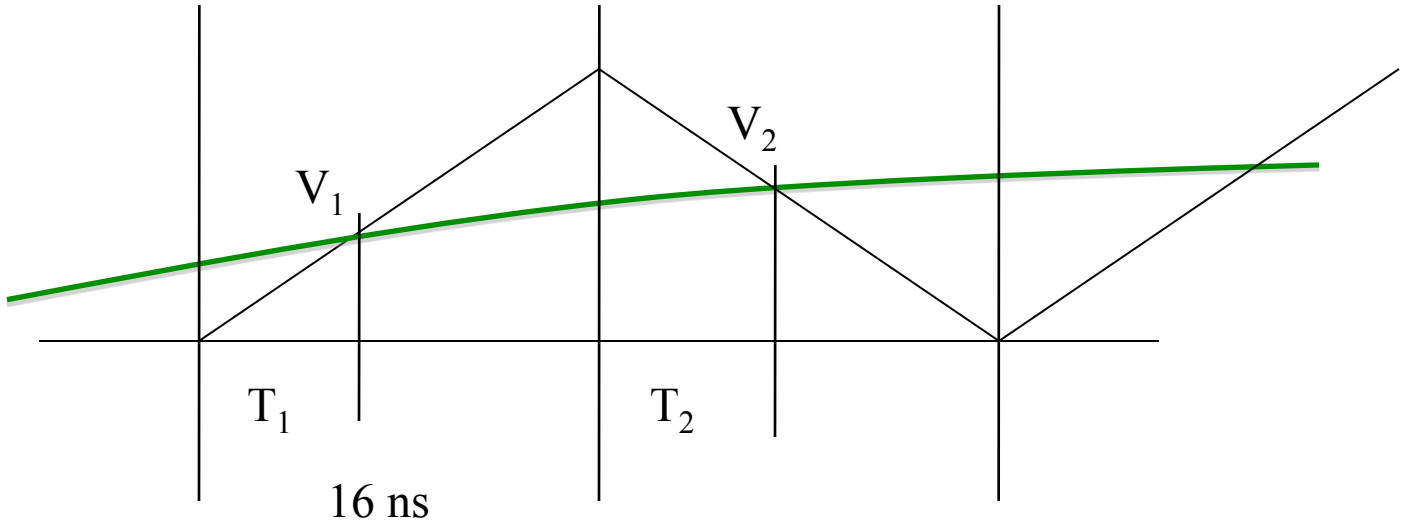
The Single Slope ADC



- Analog signal of each channel from the shaper is fed to a comparator and compared with a common ramping reference voltage V_{REF}.
- Pulses, rather than analog signals are transmitted on the cable.
- The times of transitions representing input voltage values are digitized by TDC blocks inside FPGA.
- This approach sometimes is (mistakenly) refereed as "Wilkinson ADC".

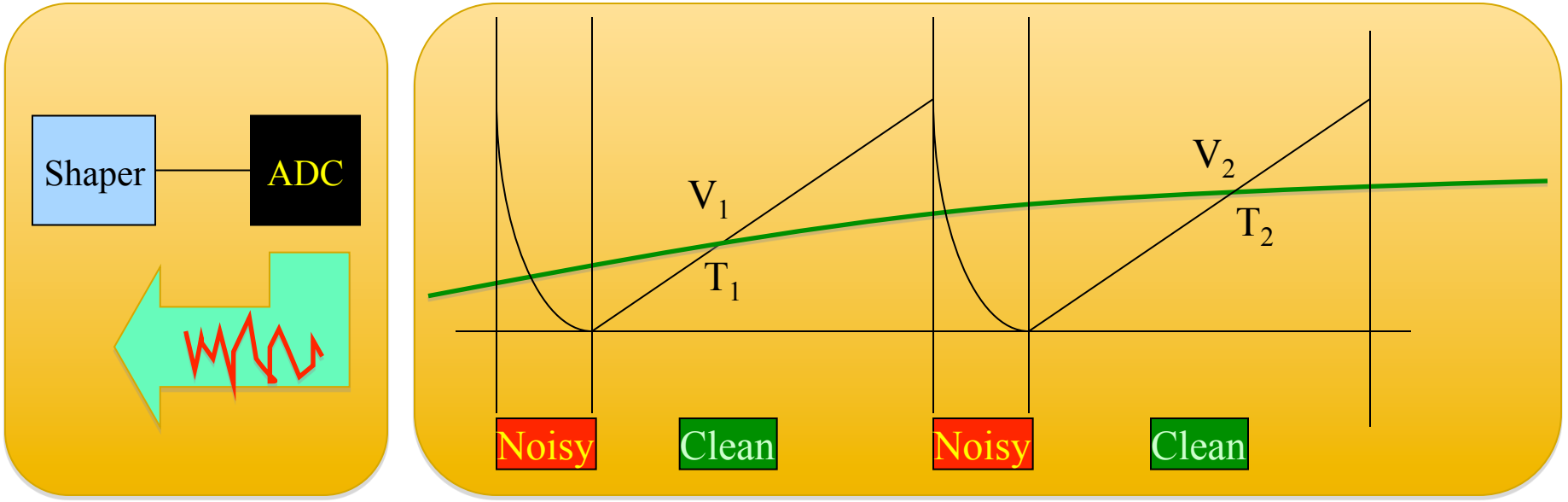


TDC Resolution Requirement



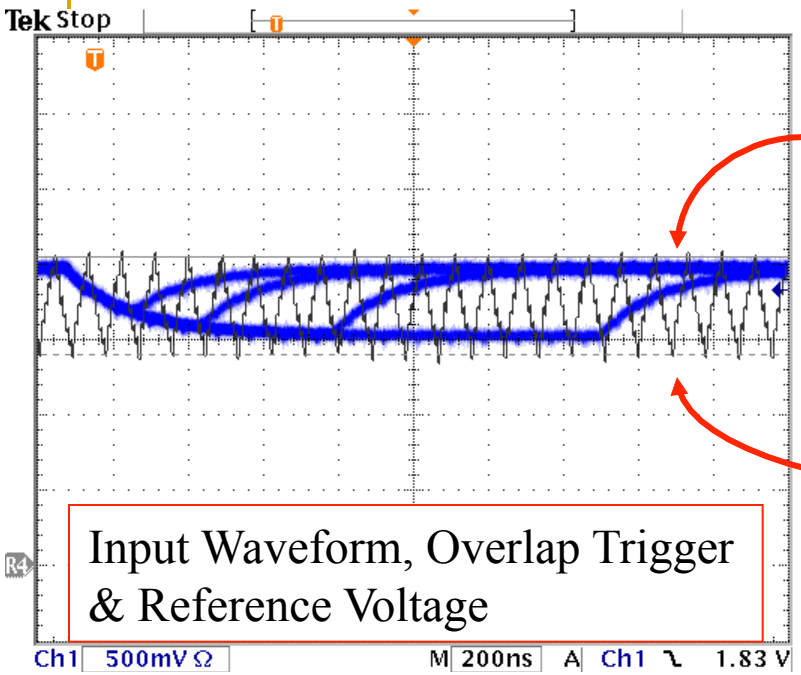
- Consider sampling rate at 62.5 MHz, the whole ramping time is 16 ns.
- To achieve 8-bit ADC precision, the TDC LSB is (16 ns)/256 = 62.5 ps.
- The low-power Wave Union TDC we implemented has an LSB < 60 ps.

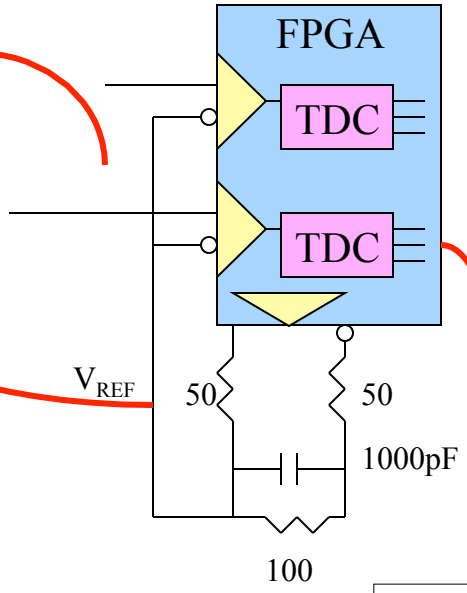
Digital Noise During Digitization



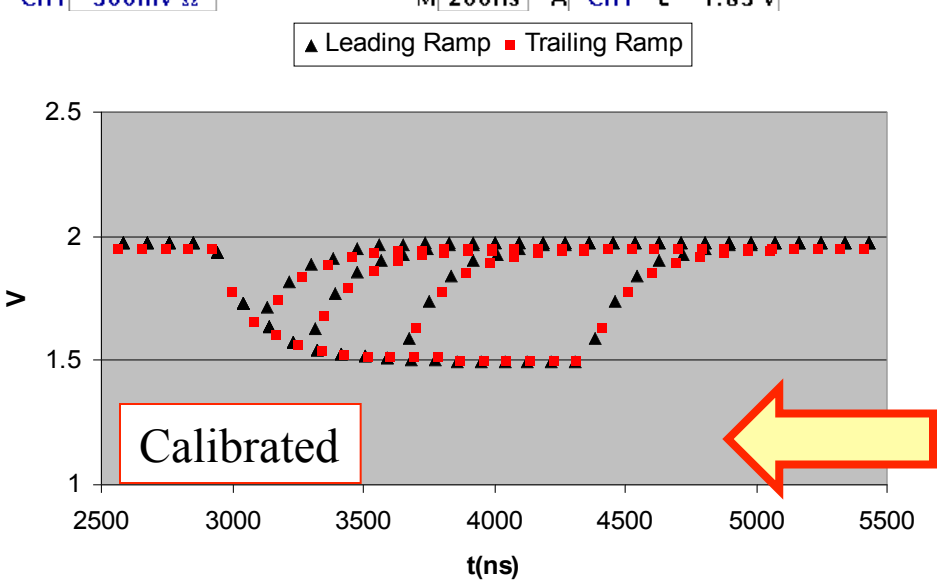
- Typical ADC devices creates noise that may interfere the analog circuits.
- The time interval for resetting of the common reference voltage may be noisy but analog signal is not sampled during it.
- There is no digital control activities during ramping up of the common reference voltage.

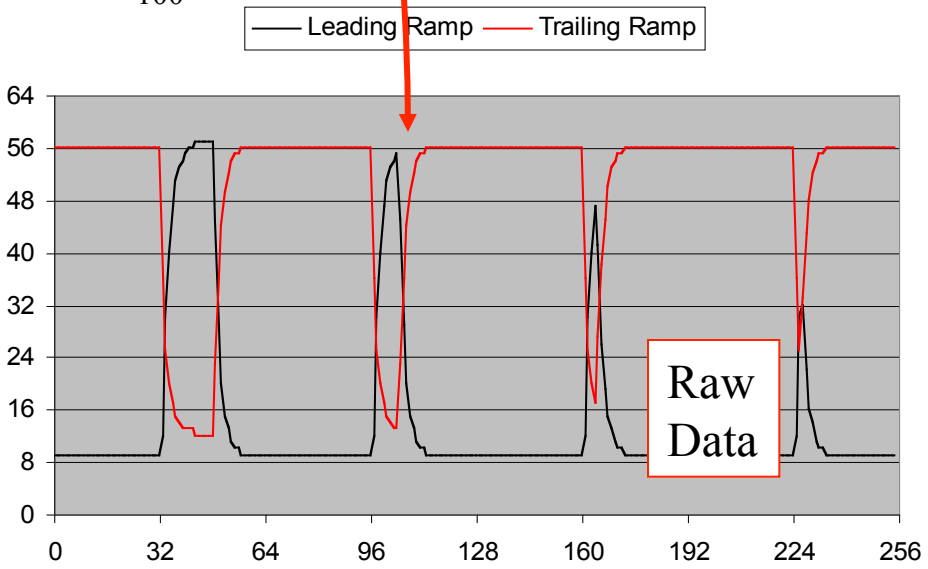
Single Slope ADC Test: Waveform Digitization



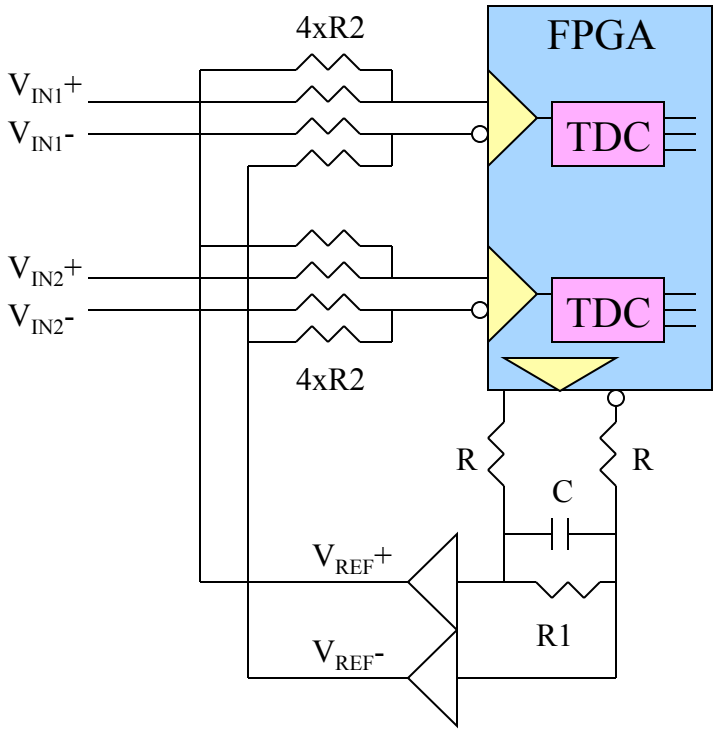


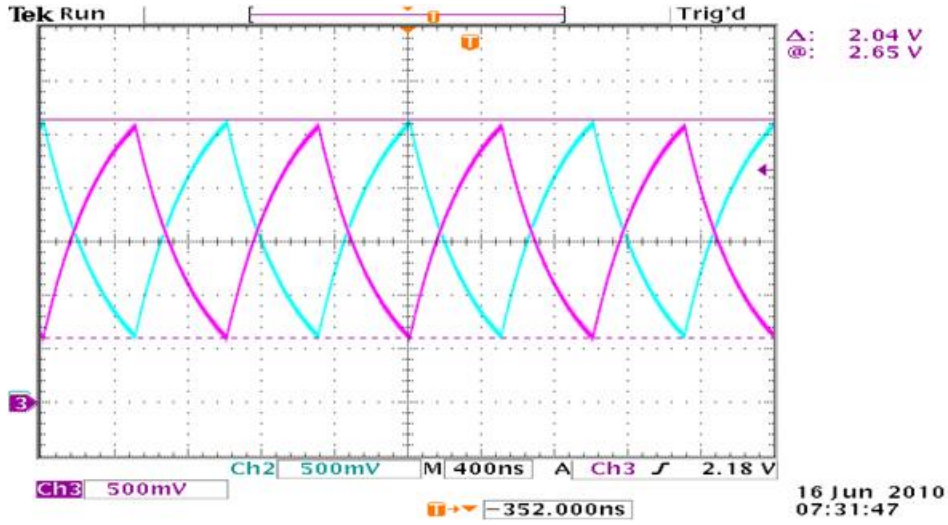
- Shown here is a demo of a 6-bit single slope TDC.
- Sampling rate in this test is 22 MHz.
- Both leading and trailing reference ramps are used in this example.
- Nonlinear reference ramping is OK. The measurement can be calibrated.

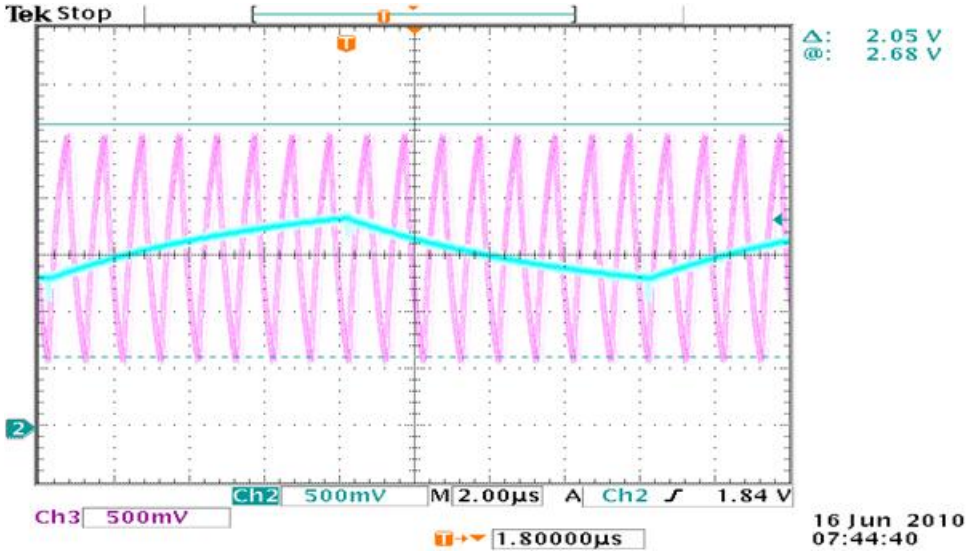




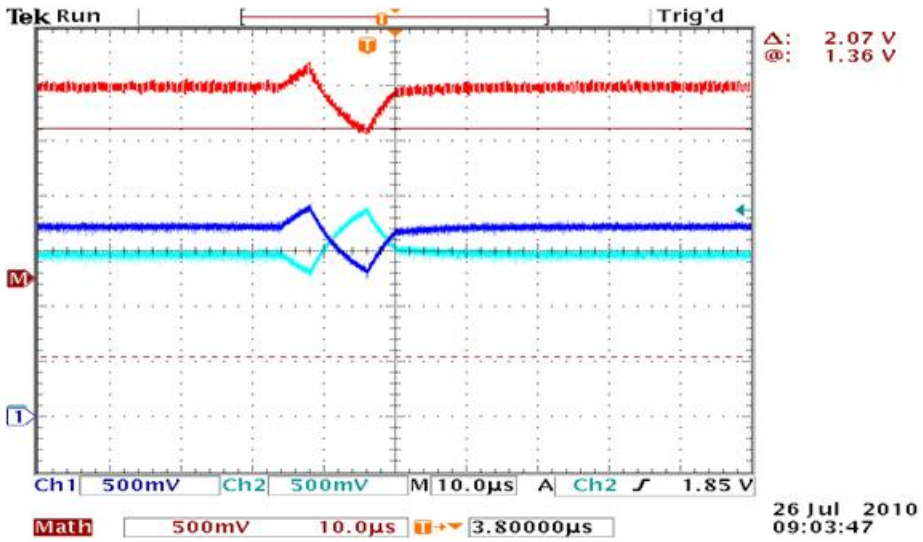
Differential Inputs and Ramping Reference Voltage

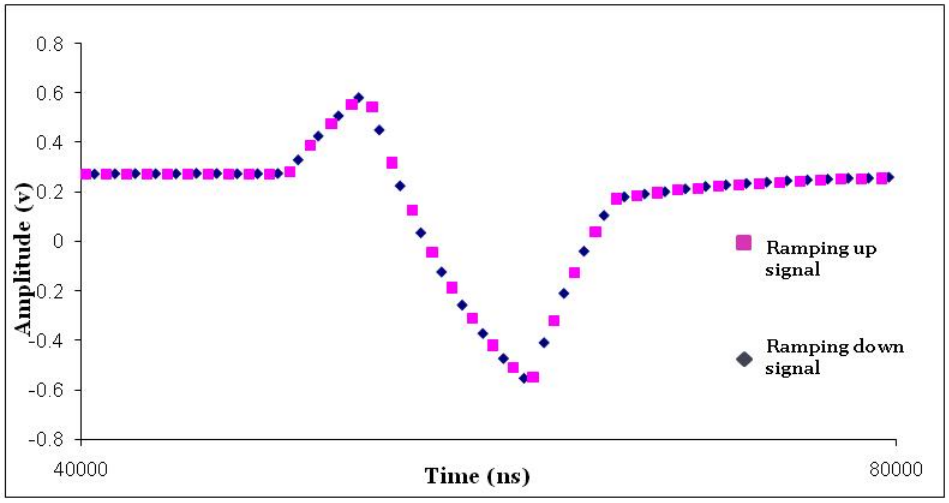




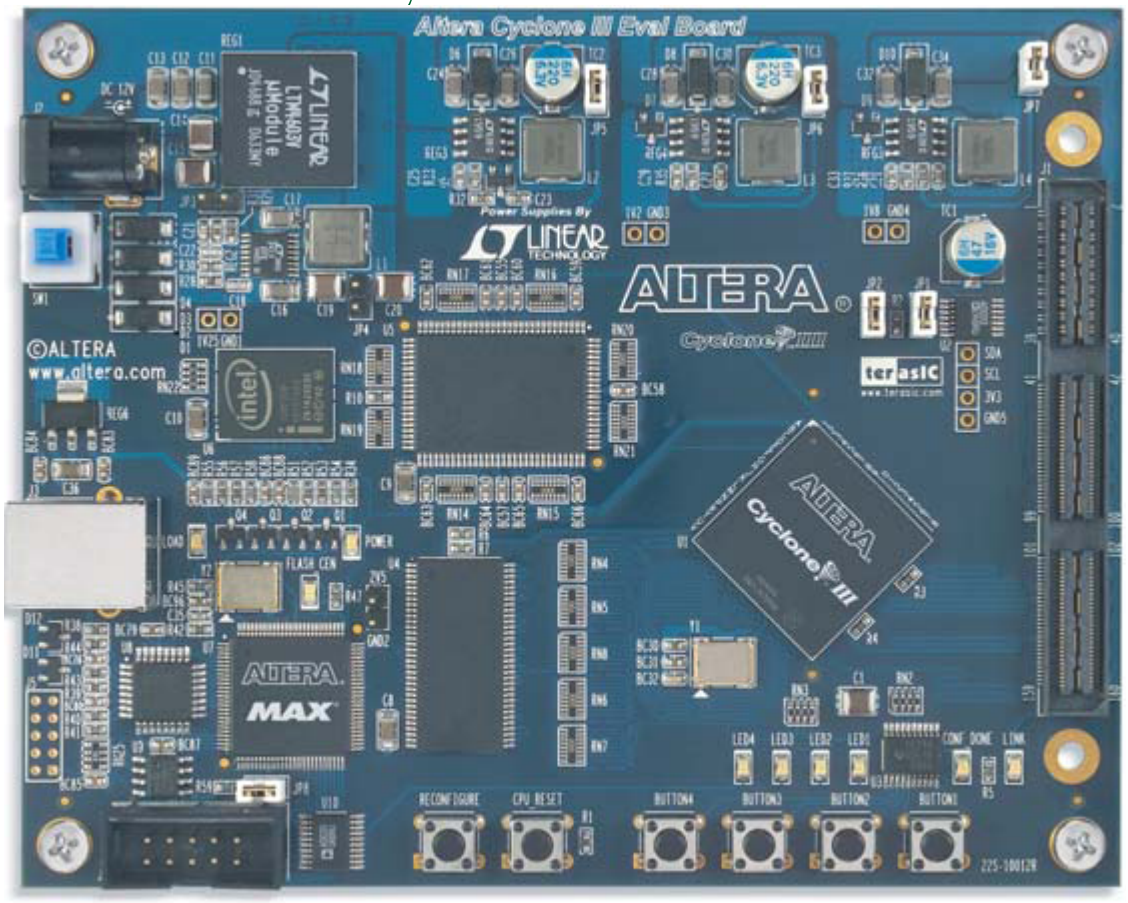


ADC Test Results



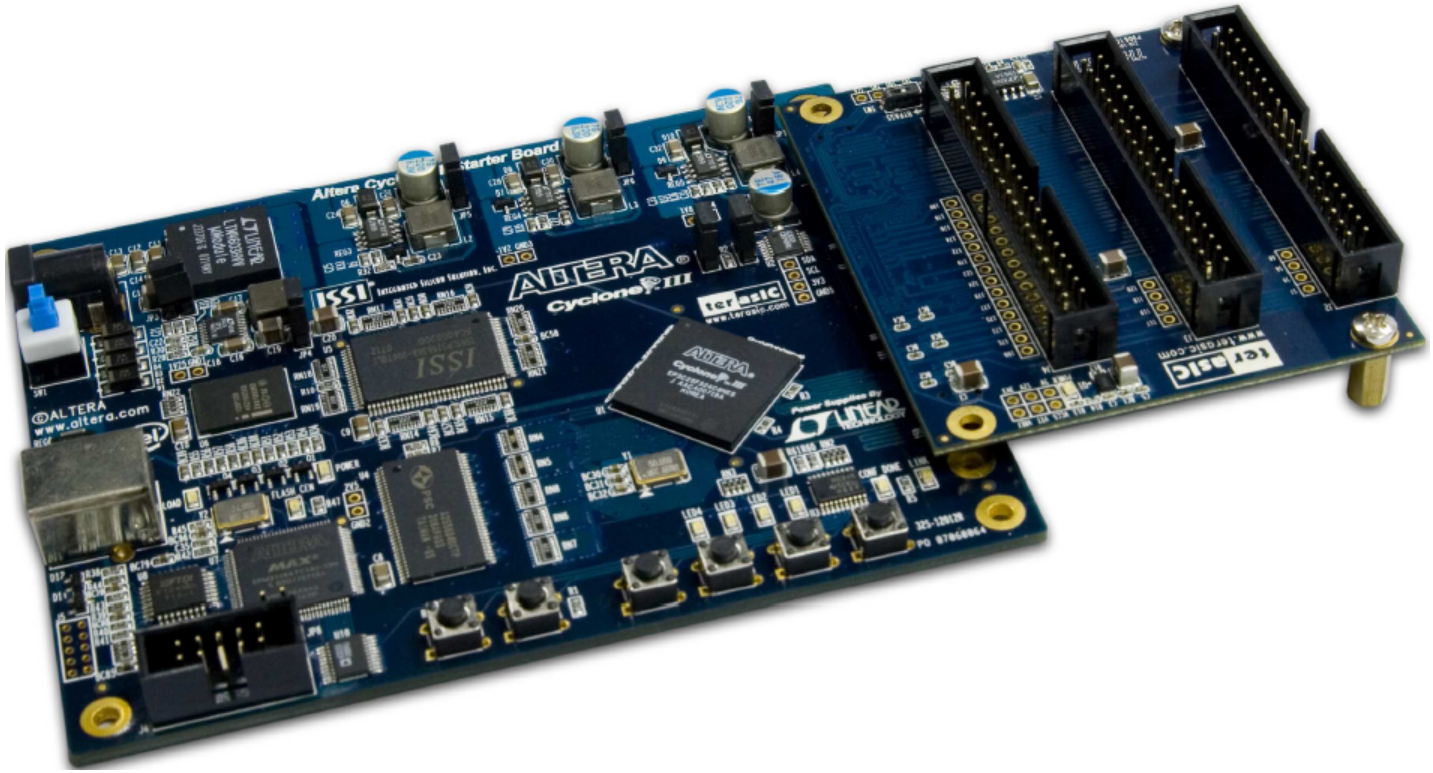


The Hardware: Cyclone III Evaluation Card



- The chip placed diagonally is the FPGA ((EP3C25F324C6N).
- The inputs come from the HSMC connector on the right.
- Hit data are stored in a RAM chip (1MB, approx. 120k hits).
- Data are read out via the USB to the host computer.

The Cyclone III Evaluation Card + Adapter Card



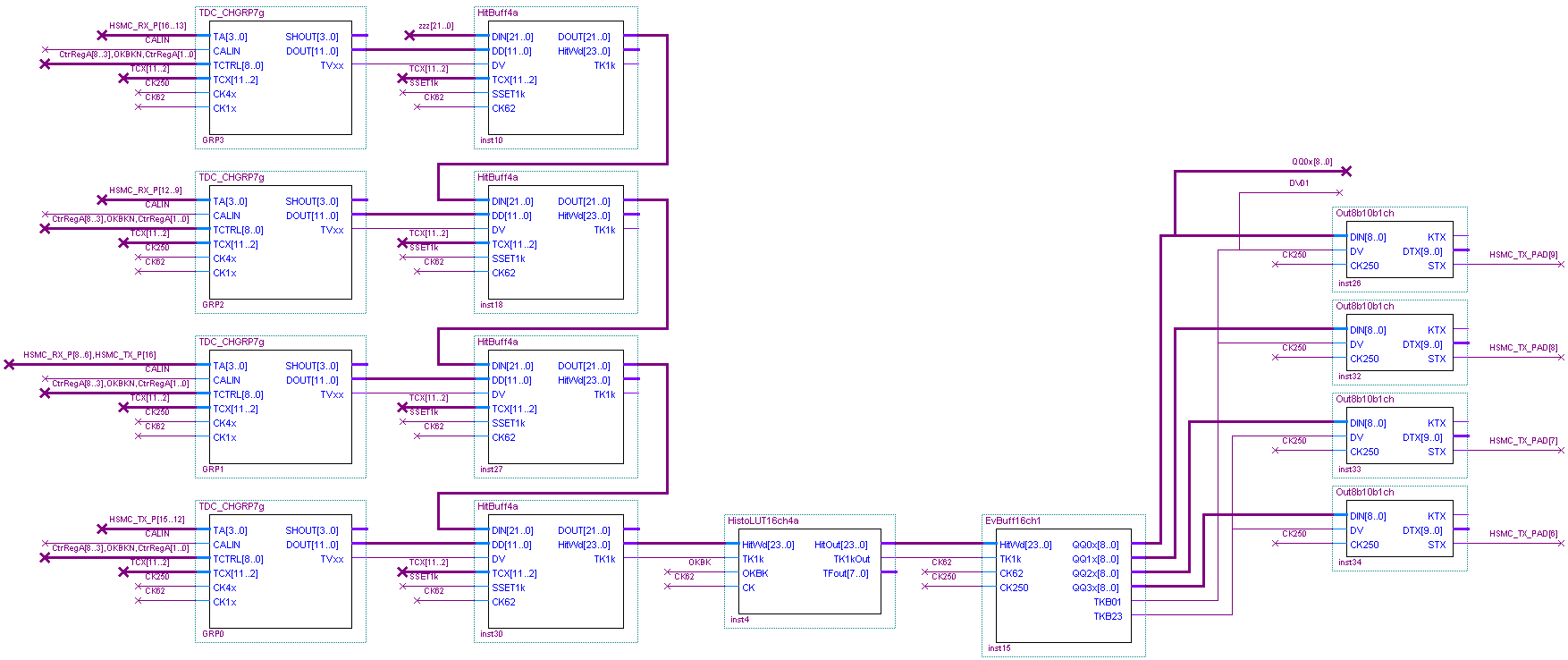
- The 16 input channel in LVDS are connected to the adapter card on the right.

Plan

- Single slope 8-bit ADC at 62.5 MHz will be tested.


The End
Thanks

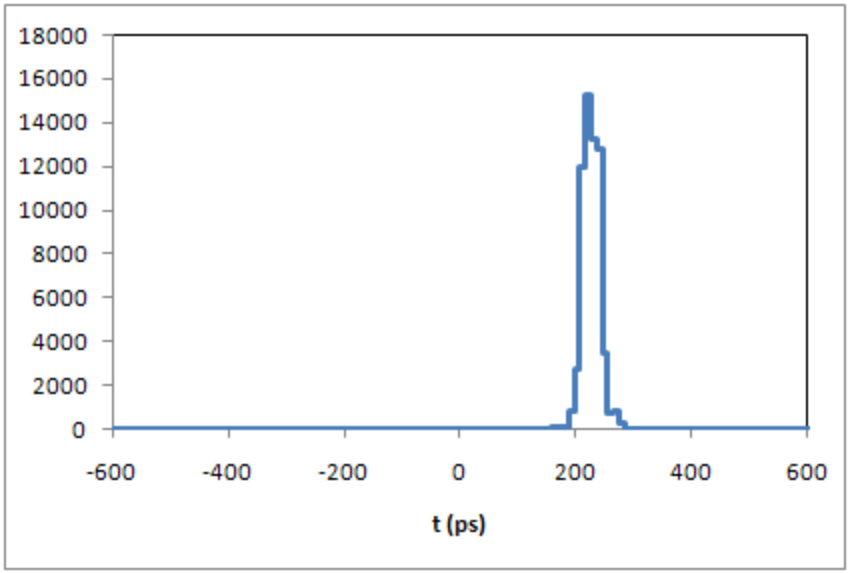
Block Diagram of 16 Channels



- The hit time for each of the 16 channel inputs is digitized and encoded.
- Data from 4 channels are buffered and data from 4 groups of 4 channels are merged together.
- Raw hit times are converted to fine time through automatic calibration block.
- Data from all 16 channels are buffered and sent out via 4 pairs of LVDS ports @250 M bits/s.

Output Raw Data and Typical Delta T Histogram Between Two Channels

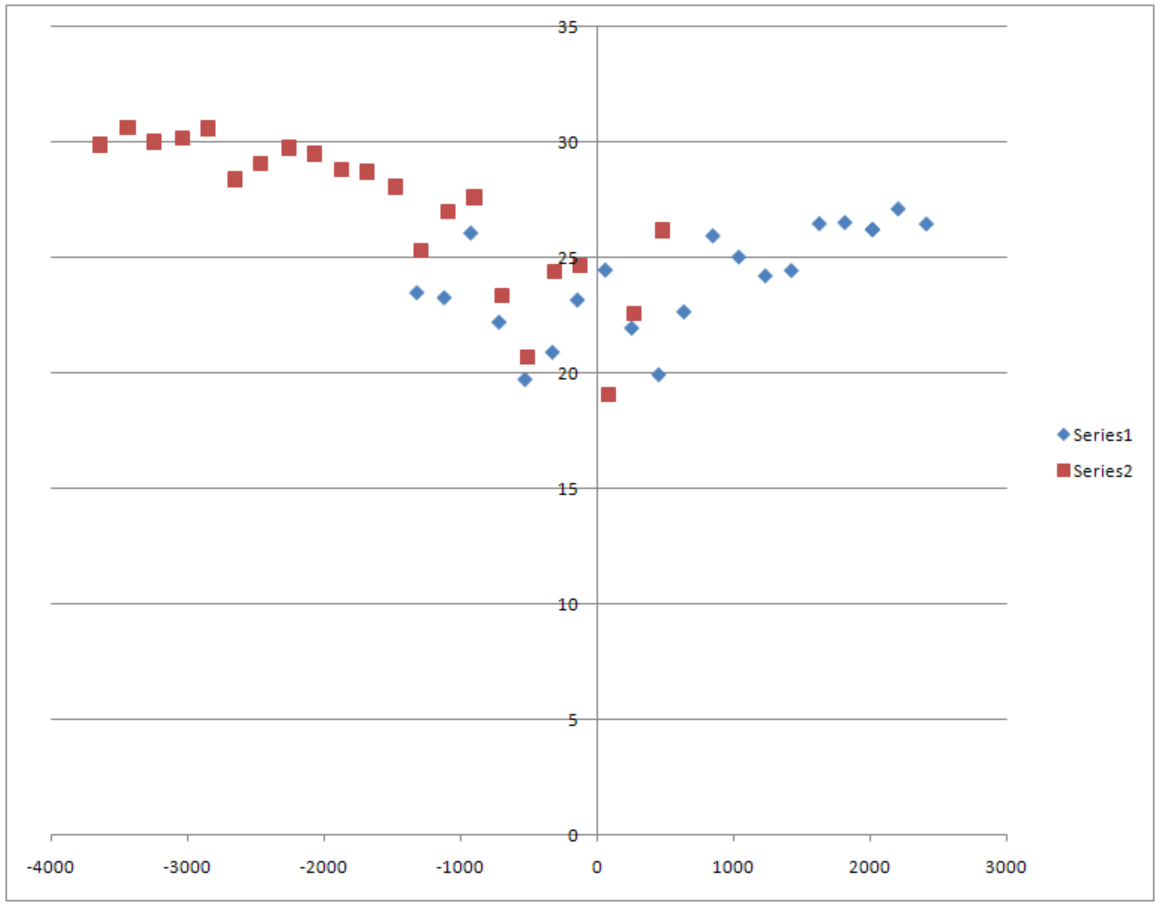
00003C
C064A6
F064B8
C07CA4
F07CB4
C094A0
F094B0
C0AC9C
F0ACAC
C0C497
F0C4A8
C0DC91
F0DCA2



- RMS of this histogram is 25 ps.

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH[3..0]				Coarse Time, LSB=4ns, TC[11..0]=96--4095, full range = 4000*4ns=16us												Fine Time, LSB=4000 ps/256=15.625ps							

Resolution at Different Time Delay

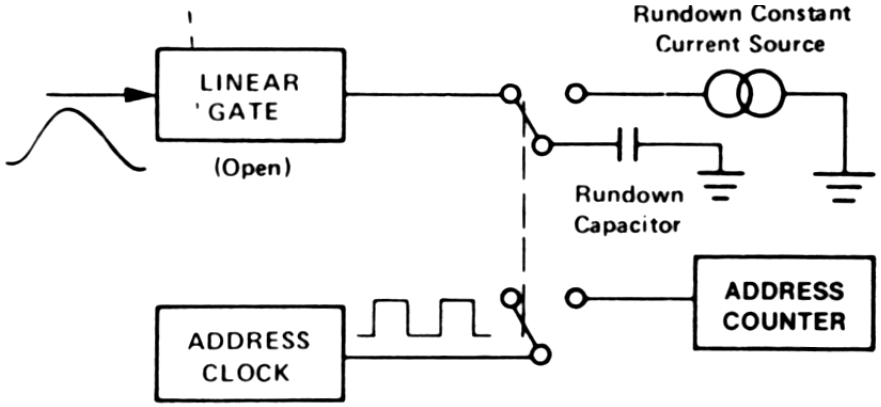


- Typical RMS resolution is 25-30 ps.
- Measurements with cleaner power (diamonds) is better than noisy power (squares).

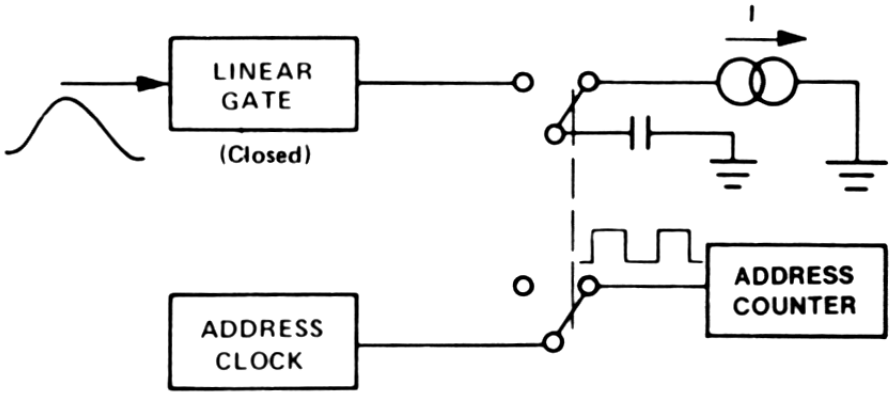
Specifications

RMS Resolution (Delta T between two channels)	30 ps
Same channel re-hit time interval	64 ns
Temporary buffer capacity	128 hits/(4 ch)/(16 us)
LVDS output port rate:	250 M bits/s/port
Output capacity in each LDVS output port:	128 hits/(16 ch)/(16 us)
Number of LVDS output ports:	1, 2, 3, 4/(16 ch)

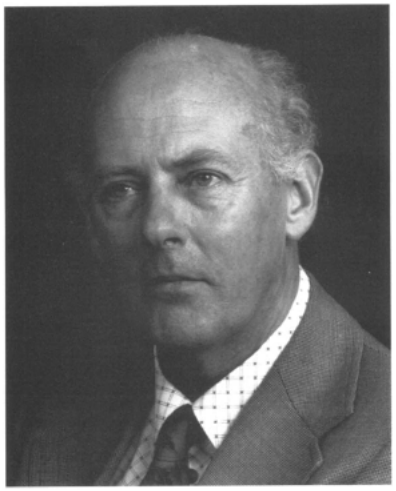
The Wilkinson ADC



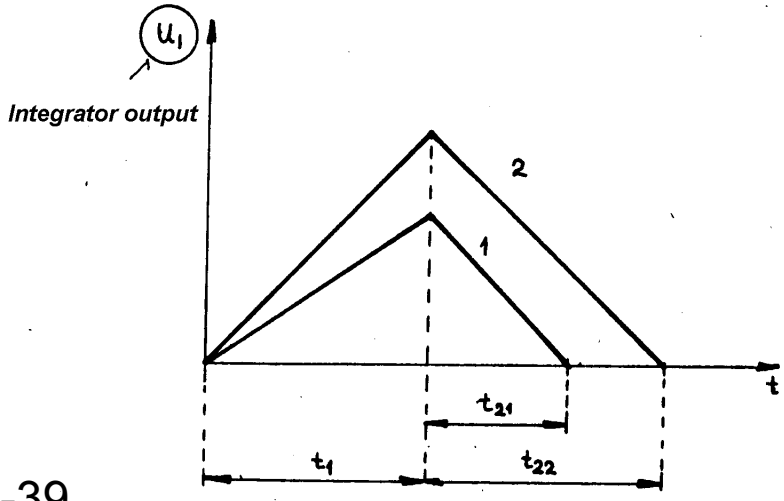
(a) Capacitor Charging



(b) Capacitor Rundown



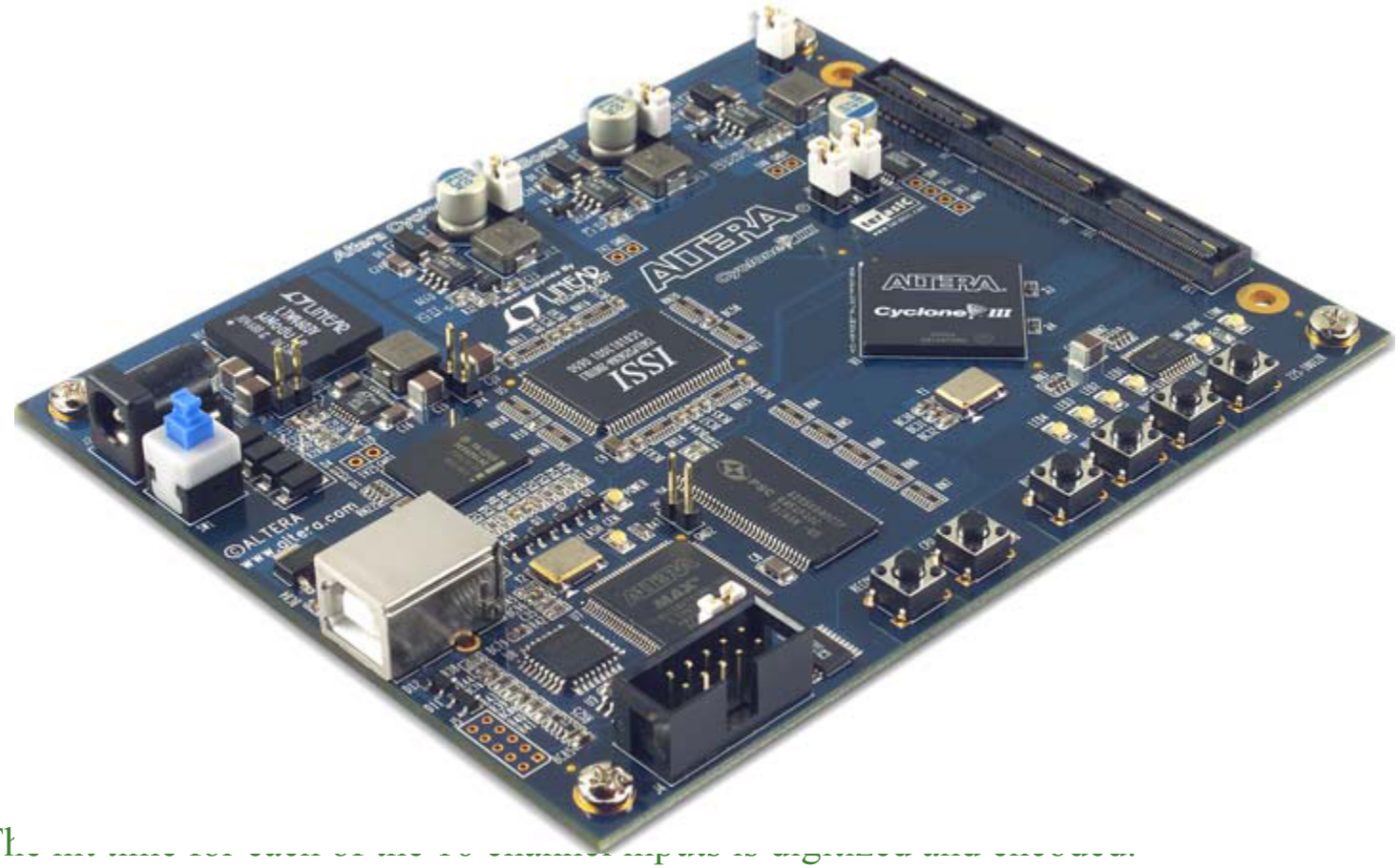
Denys Wilkinson



Ref: Annu. Rev. Nucl. Part. Sci. 1995.45.'1-39

http://www.dnp.fmph.uniba.sk/~kollar/je_w/el3.htm

The Hardware: Cyclone III Evaluation Card



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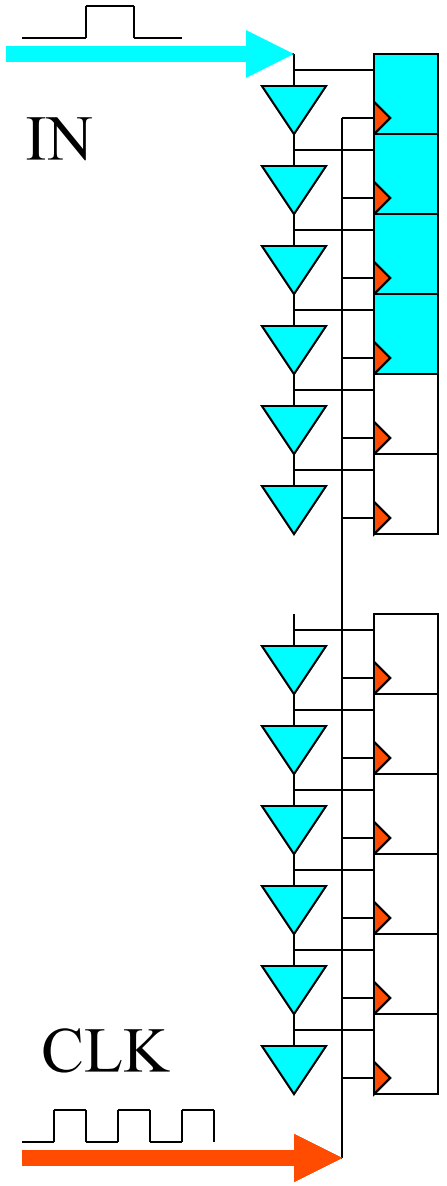
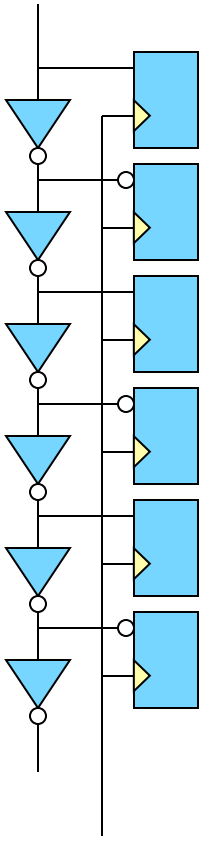
TDC Implemented with FPGA

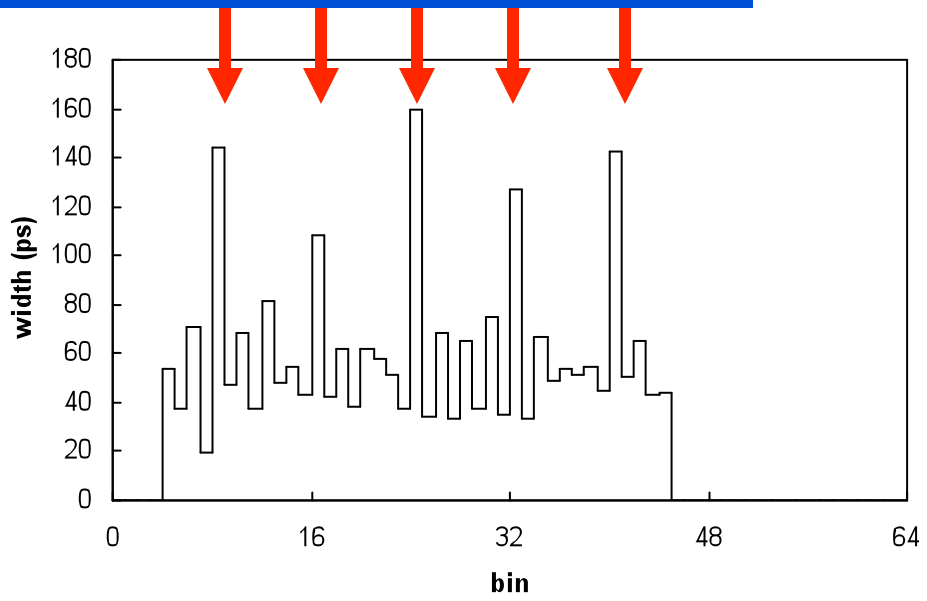
TDC Using FPGA Logic Chain Delay



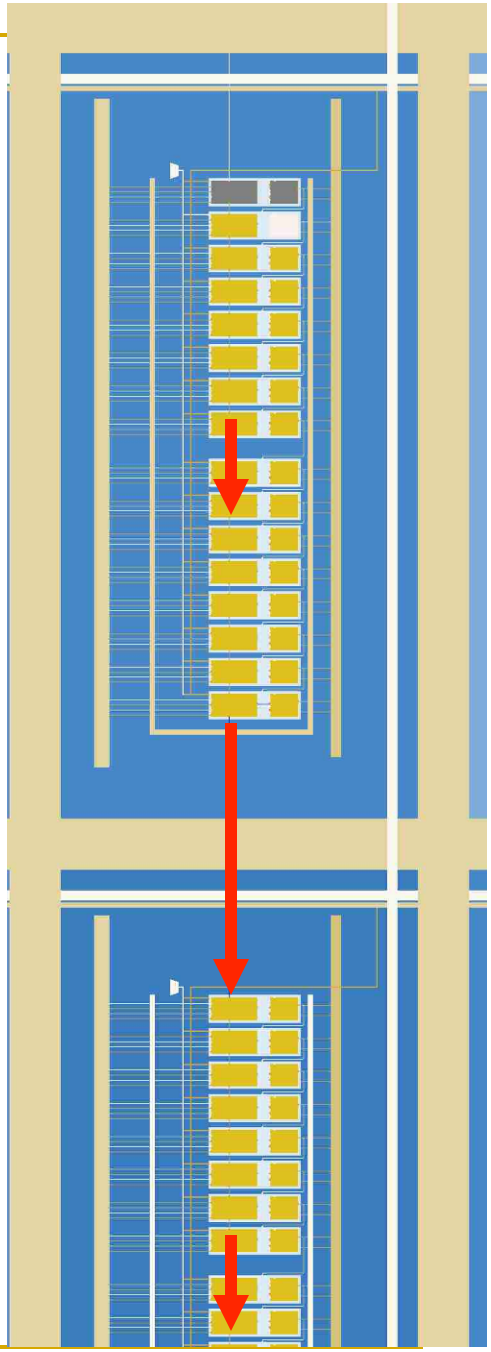
- This scheme uses current FPGA technology ☺
- Low cost chip family can be used. (e.g. EP2C8T144C6 $31.68) ☺
- Fine TDC precision can be implemented in slow devices (e.g., 20 ps in a 400 MHz chip). ☺

Two Major Issues In a Free Operating FPGA

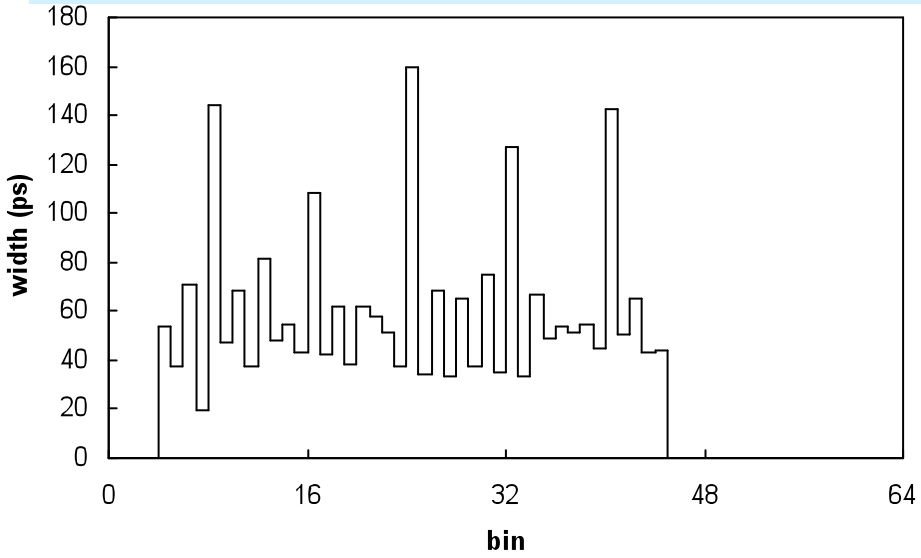


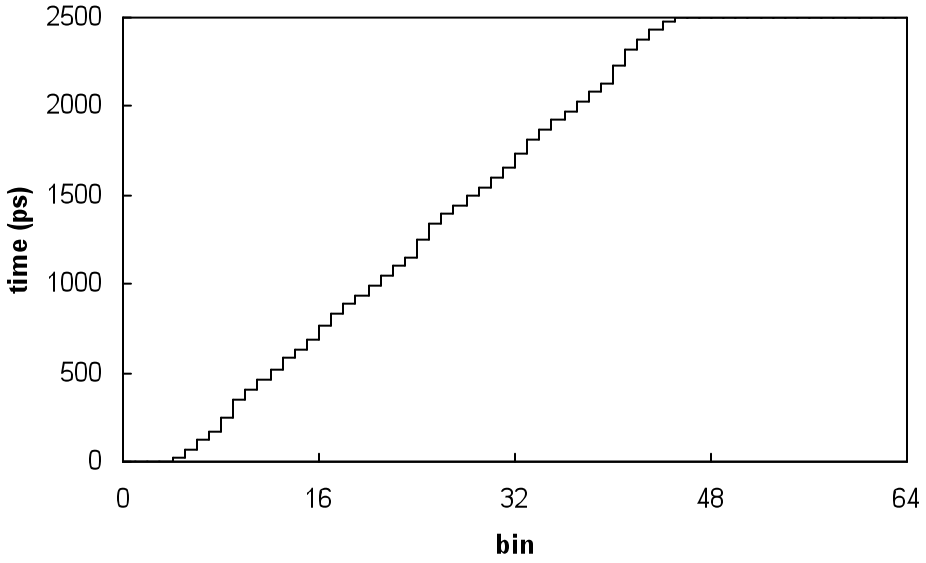


1. Widths of bins are different and varies with supply voltage and temperature.
2. Some bins are ultra-wide due to LAB boundary crossing

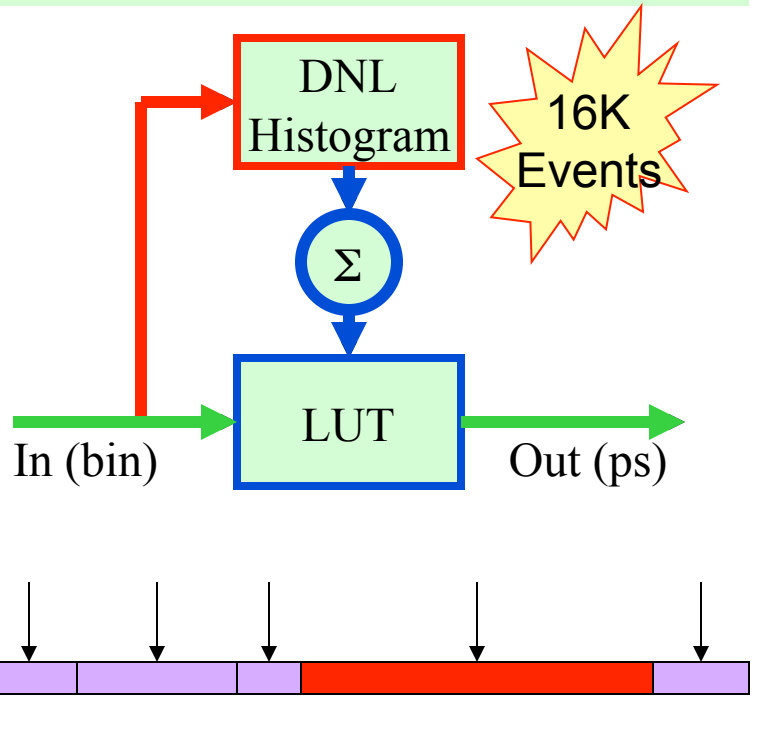


Auto Calibration Using Histogram Method

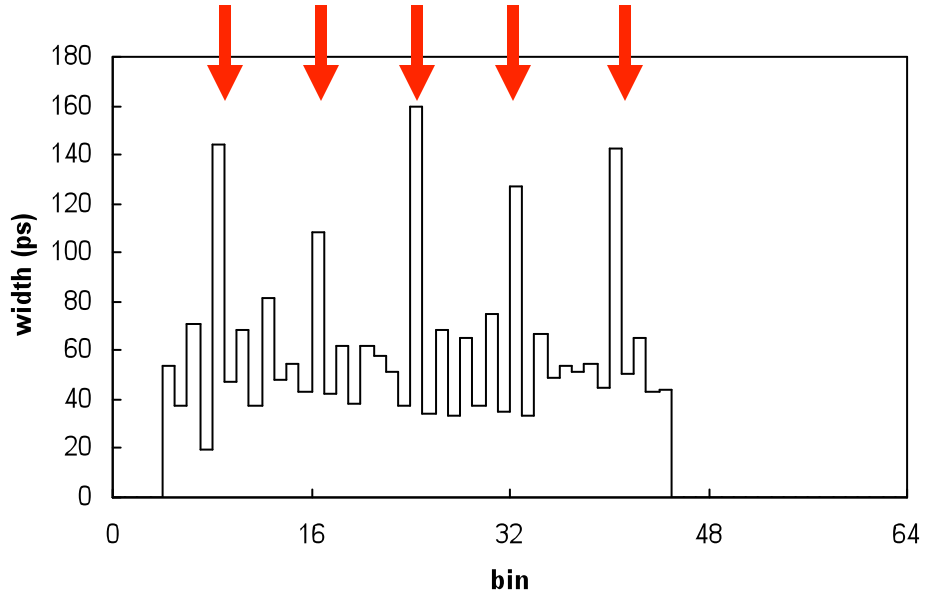




- It provides a bin-by-bin calibration at certain temperature.
- It is a turn-key solution (bin in, ps out)
- It is semi-continuous (auto update LUT every 16K events)

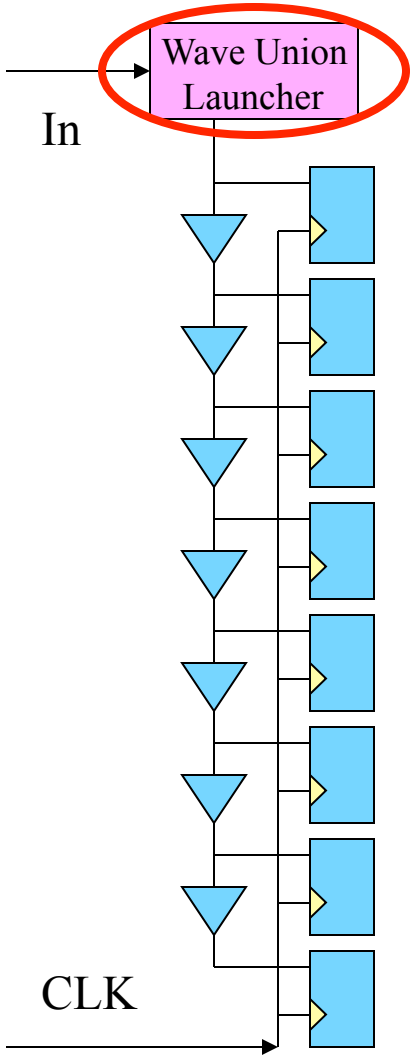


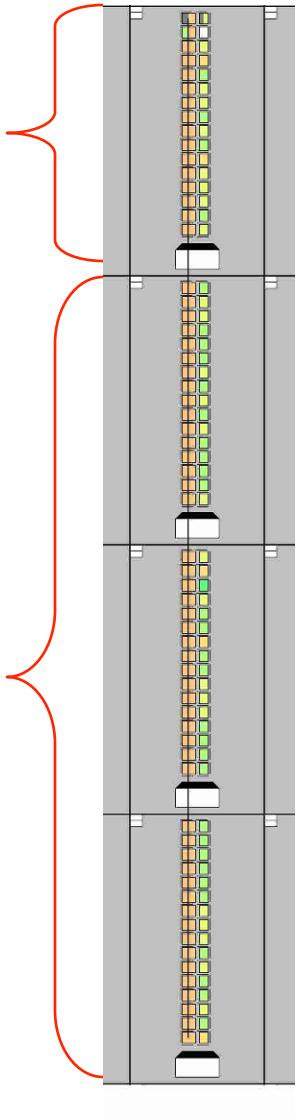
Good, However



- Auto calibration solved some problems ☺
- However, it won't eliminate the ultra-wide bins ☹

Cell Delay-Based TDC + Wave Union Launcher





The wave union launcher creates multiple logic transitions after receiving a input logic step.

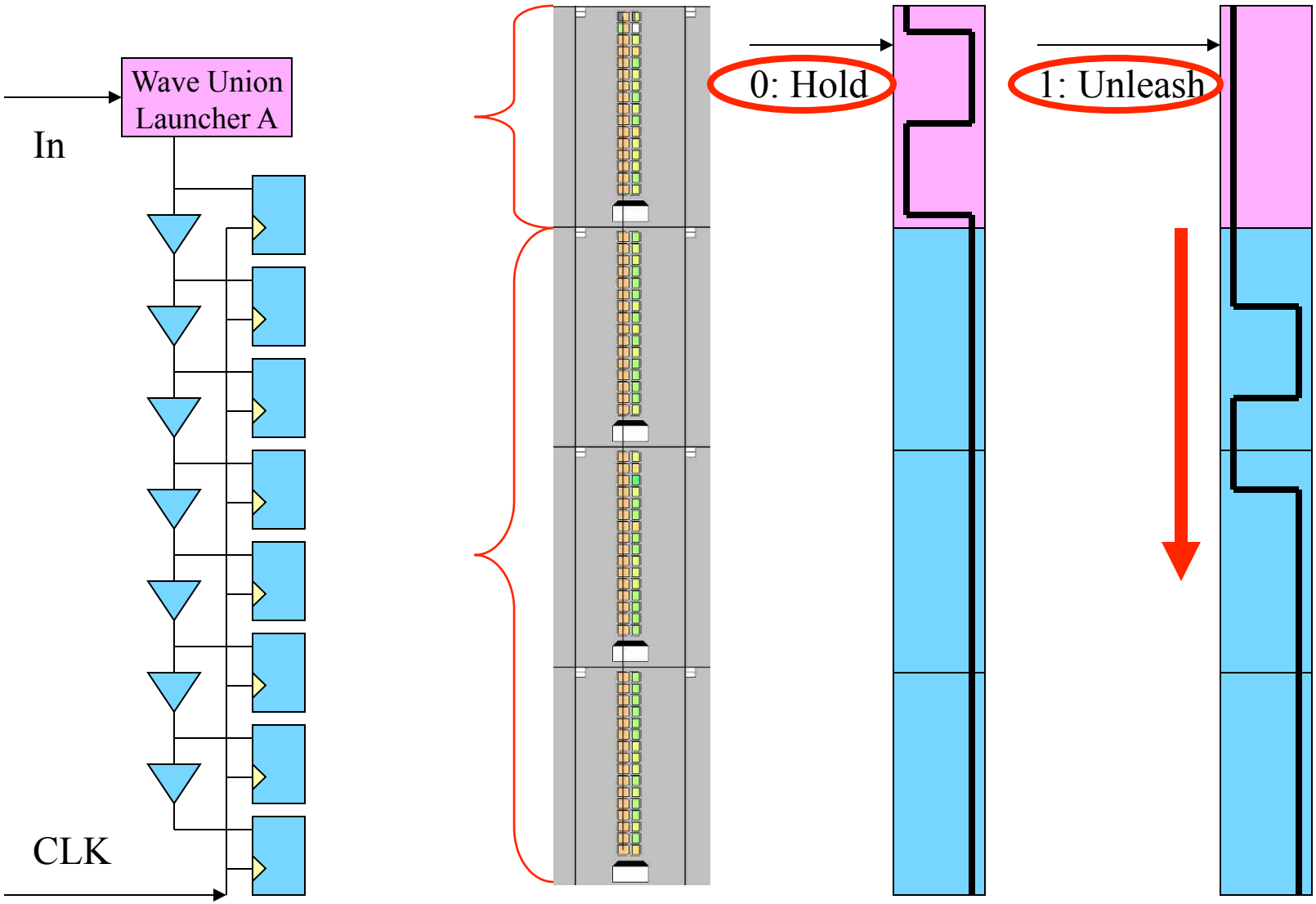
The wave union launchers can be classified into two types:

- Finite Step Response (FSR)
- Infinite Step Response (ISR)

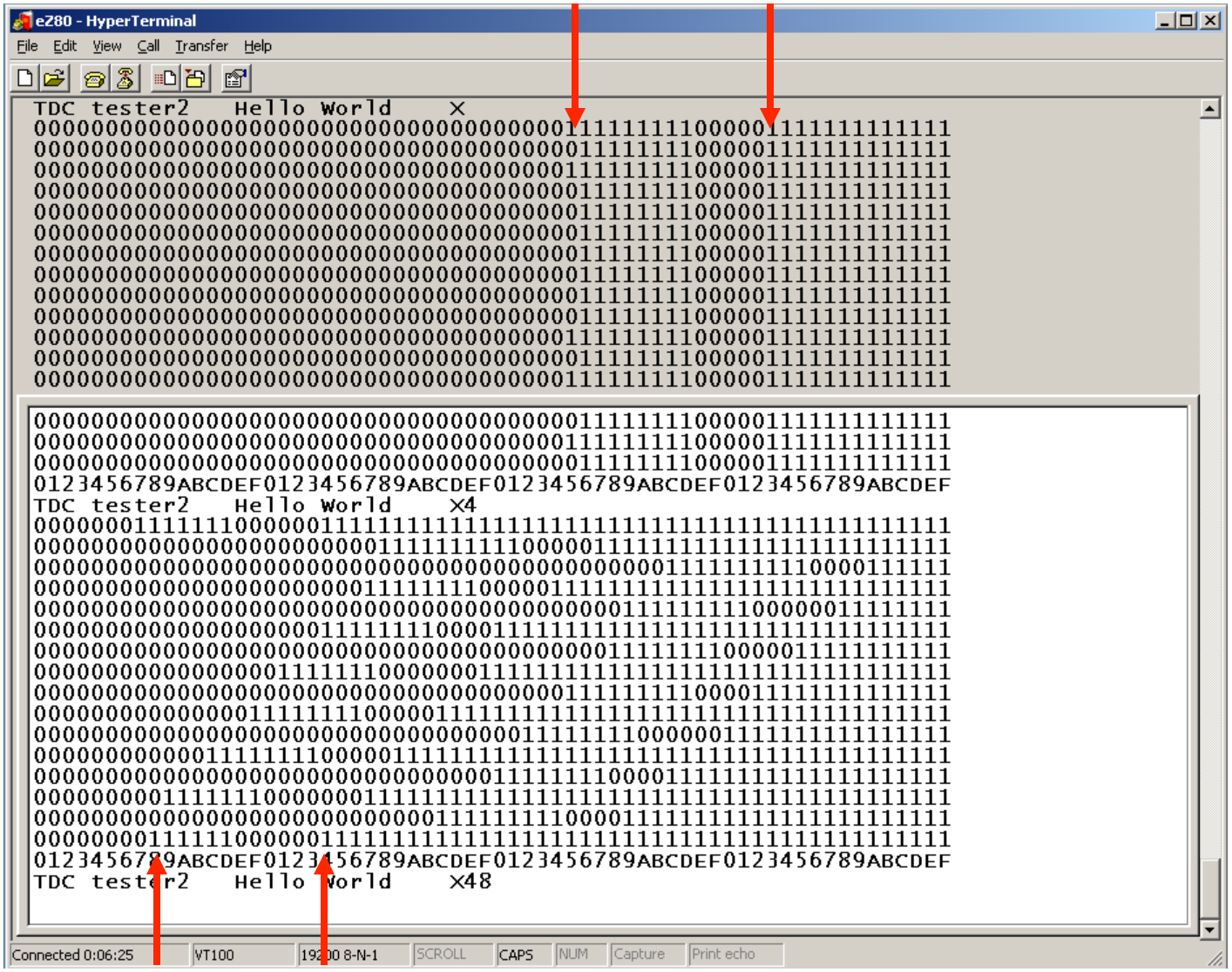
This is similar as filter or other linear system classifications:

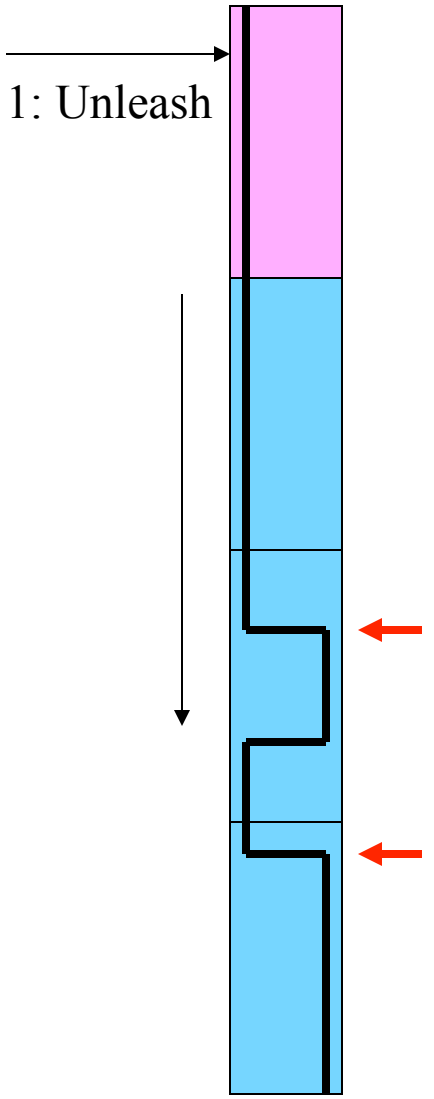
- Finite Impulse Response (FIR)
- Infinite Impulse Response (IIR)

Wave Union Launcher A (FSR Type)

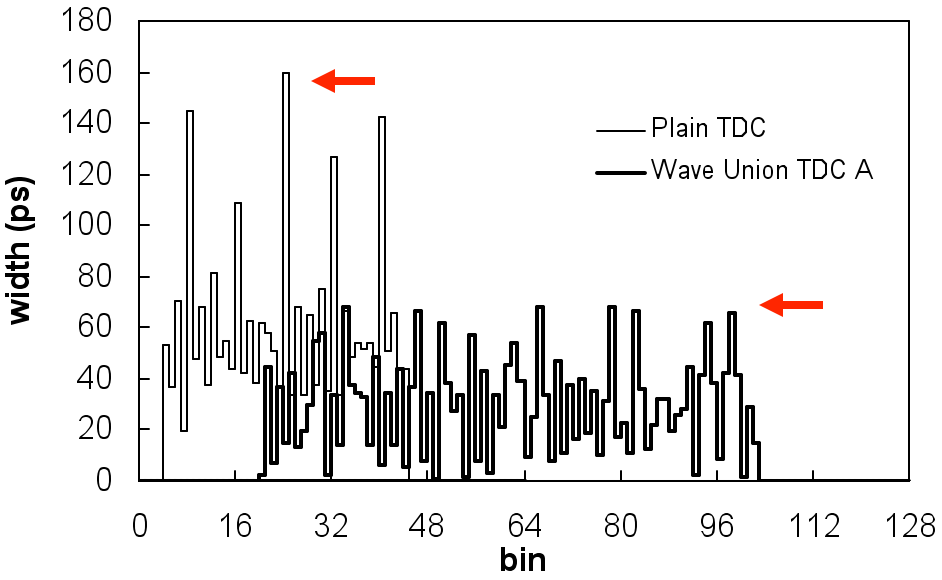


Wave Union Launcher A: *2 Measurements/hit*





Sub-dividing Ultra-wide Bins



Device: EP2C8T144C6

- Plain TDC:
  - Max. bin width: 160 ps.
  - Average bin width: 60 ps.
- Wave Union TDC A:
  - Max. bin width: 65 ps.
  - Average bin width: 30 ps.